Proceedings of the 2003 IEEE International Frequency Control Symposium and PDA Exhibition
Jointly with the 17th European Frequency and Time Forum

PHASE NOISE REDUCTION IN SURFACE WAVE OSCILLATORS BY USING NONLINEAR SUSTAINING AMPLIFIERS

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Abstract - **Nonlinear sustaining amplifier operation has been investigated and applied to high-power negative resistance oscillators (NRO), using single-port surface transverse wave (STW) resonators, and two-transistor sustaining amplifiers for feed-back-loop STW oscillators (FLSO) using lossy two-port STW devices. In all cases, self limiting Si-bipolar sustaining amplifiers which operate in the highly nonlinear AB-, B- or C-class modes are implemented. Phase noise reduction is based on the assumption that a sustaining amplifier, operating in one of these modes, uses current limiting and remains cut off over a significant portion of the wave period. Therefore, it does not generate 1/f noise over the cut-off portion of the RF cycle and this reduces the close-in oscillator phase noise significantly. The proposed method has been found to provide phase noise suppression levels in the -111 to -119 dBc/Hz range at 1 KHz carrier offset in 915 MHz C-class power NRO and FLSO generating up to 23 dBm of RF-power at RF/dc efficiencies exceeding 40%. C-class amplifier design techniques are utilized for adequate matching and high RF/d.c. efficiency.**

I. INTRODUCTION

Although substantial effort has been made to improve surface acoustic wave (SAW) oscillator performance over the last three decades [1], designing a simple and inexpensive SAW oscillator, featuring low phase noise, high efficiency and, therefore, low heat dissipation at a low supply voltage, remains a serious challenge. Very few companies offer high-performance SAW oscillators in which low phase noise is achieved with highly sophisticated designs and using modular amplifiers, specially selected for low 1/f noise. The efficiency of such oscillators rarely exceeds a few percent, they are bulky, dissipate a lot of heat and, finally, at a price exceeding $1000,-/pcs. their mass application is very limited. On the other hand, a variety of low-cost SAW oscillators are available mainly for keyless entry and security systems and applications in optical communication networks. Their phase noise performance is generally very poor and tailored just to meet the requirements of a specific application. Such oscillators rarely take advantage of the remarkable phase noise performance and efficiency achievable with SAW oscillator technology. In the author's opinion, the main reason for this situation is that oscillator design engineers believe that mainly the Q of the SAW device is responsible for the oscillator's phase noise and rarely consider the fact that, at a given oscillator Q, the sustaining amplifier and its nonlinear operation can significantly improve or degrade the phase noise performance [2]. SAW-oscillator noise is predicted by using Leeson's model [1] which works well in FLSO with nearly linear operation and a constant 1/f contribution of the sustaining amplifier. This model, however, does not take into account nonlinear issues like gain compression, current or voltage limiting or class of the sustaining amplifier operation. This is the reason why, in practical, oscillators the predicted by Leeson's model phase noise performance agrees with the measured one only if, first: the sustaining amplifier is ideally linear and features perfect limiting characteristics and, second: the 1/f noise performance of the SAW device, sustaining amplifier and other active circuits in the loop is known and does not change when the oscillator loop is closed. Practically, in most cases, such idealistic conditions are achievable with low-efficiency A-class sustaining amplifiers, automatic level control (ALC) circuits and external limiters. This complicates the entire design and introduces additional 1/f noise from external active devices [3].

This paper describes simple STW low-phase-noise oscillators whose sustaining amplifiers operate in highly nonlinear classes of operation such as AB, B and C. Close-to-carrier phase noise reduction is based on the fact that, a transistor, operating in one of these modes, uses current limiting and remains cut off over a significant portion of the wave period. Therefore, while cut off, it does not generate 1/f noise. If such a transistor is used as a sustaining amplifier in an oscillator, then its phase noise will be proportional to the conduction angle θ, measured in radians or degrees, or in percent, referenced to the full 2π angle at A-class operation. Therefore, the lower θ, the lower the phase noise. For the first time, this principle was successfully applied to a low-cost STW based FLSO in [2]. Here, it will be further investigated and also applied to STW-based NRO stabilized with single-port resonators and to two-transistor based FLSO stabilized with lossy two-port devices. An additional effect of nonlinear sustaining amplifier operation is its high efficiency. Theoretically, the amplifier efficiency can approach 100% in C-

class operation [4]. As shown in this work, in practical SAW oscillators RF/dc efficiencies in the 40 to 50% range are achievable.

II. Nonlinear Amplifier Operation

A. Classification of Nonlinear Amplifiers

The sustaining amplifier in an oscillator is a power amplifier (PA) circuit converting dc-input power into a significant amount of RF/microwave power [5]. PAs are designated as classes A-F which differ in the method of operation, efficiency and power-output capability [5]. Here, we will consider only A, B, AB and C class of operation since they are relevant to the oscillator circuits subject of this study. Fig. 1 describes the basic Si-bipolar transistor circuit operating in one of these classes. A dc bias voltage and a drive signal are applied to the transistor's base. This causes an oscillating collector current Ic to flow from the dc supply voltage Us and deliver a substantial amount of power to the load resistor R_{load}. The output filter provides optimum matching to the load at the desired frequency and suppresses unwanted harmonics. The four different classes of operation are described in Fig. 2 a) through d). In the A-class mode (see Fig. 1 a)), the transistor is biased at a collector current $I_c=I_{cbias}$ in the active region and remains conducting over the entire wave period. The drive signal modulates I_c between I_{cmin} and I_{cmax} but the average current remains constant and equal to I_{cbias}, regardless of whether a drive signal is applied or not. Since the input and output wave forms are sinusoids and I_c is modulated over its linear region, the amplification is high and linear and the output voltage across R_{load} can never exceed Us. This is why the maximum theoretical A-class collector efficiency can never exceed 50% [5].

In the AB-class mode, the transistor is slightly forward biased and remains cut off over part of the negative half of the duty cycle. This cut-off region during which $I_c=0$, is shown by the shaded area in Fig. 2 b).

In the B-class mode, the transistor base is set to 0V dc. A current flow and amplification will occur only during the positive part of the duty cycle as shown in Fig. 2 c) and

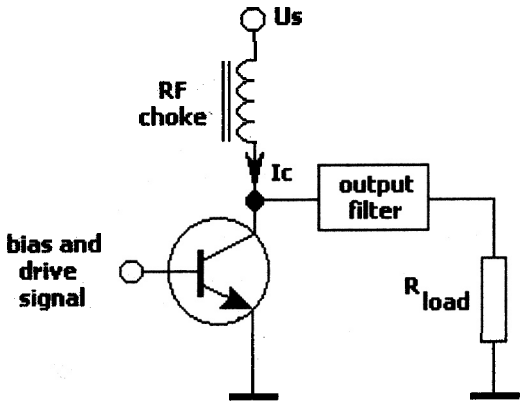

Fig. 1. Basic PA transistor circuit for one of the A, AB, B and C-classes of operation.

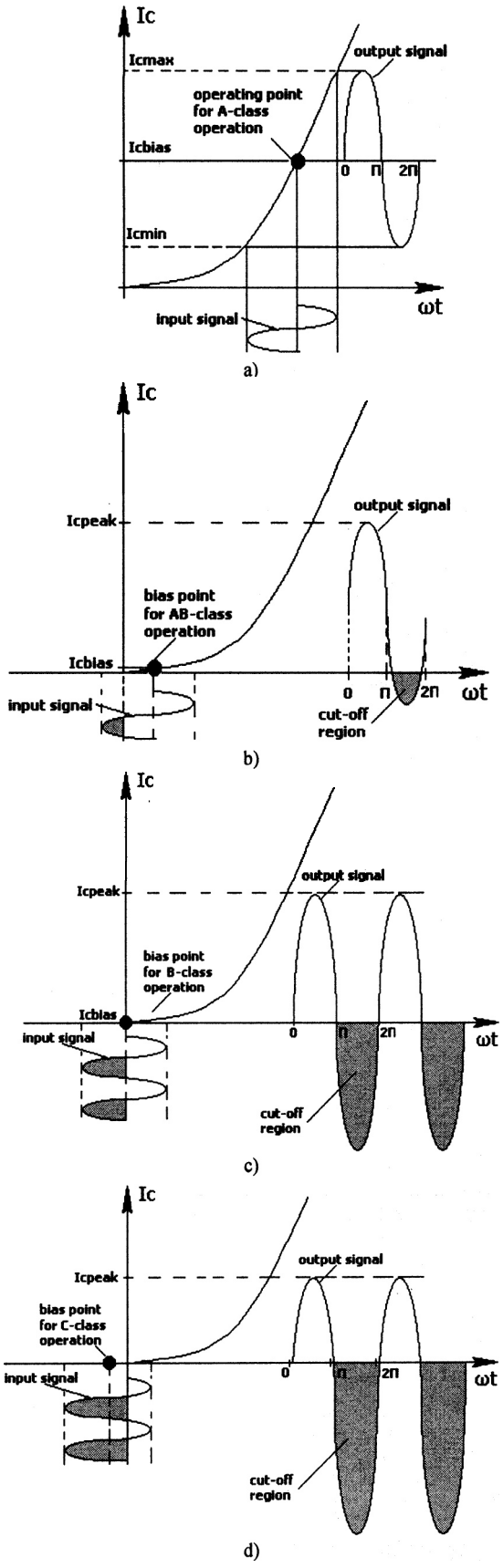

Fig. 2. PA classes of operation: a): A class; b): AB class; c): B class and d): C class.

θ=180 deg. The maximum theoretical collector efficiency is 78.5% [5].

In the C-class of operation, the transistor is biased for a θ<180 deg. as shown in Fig. 2 d). The collector current waveform is a sequence of narrow pulses and far from linear. Theoretically, if θ is reduced towards zero, the efficiency can reach 100% [5].

B. Nonlinear Operation, 1/f Noise and Efficiency

This study assumes that the sustaining PA is the dominant source of 1/f noise in the oscillator [1]. If the assumption that the PA does not generate 1/f noise when no collector current flows through it is true, then the sustaining amplifier will noise modulate the carrier only during the conducting part of the duty cycle. Therefore, the PA 1/f noise contribution will be proportional to θ and the single-side-band phase noise reduction *NR*, measured in dB, will be:

$$NR=20\log(\theta/2\pi) \quad (1)$$

In an A-class sustaining amplifier noise modulation will occur over the entire 360 deg. duty cycle duration and *NR* will be 0. In case of a B-class sustaining amplifier with θ=50% and a C-class amplifier with θ=10% of the duty cycle, a 6 and 20 dB noise reduction, respectively, should occur. The main idea of this study is, by moving from the linear A-class operation to one of the nonlinear AB, B or C classes of sustaining amplifier operation, to reduce the phase noise and increase the RF/dc efficiency of a SAW/STW resonator stabilized oscillator. The expected phase noise reduction and oscillator efficiency as a function of the conduction angle is summarized in Table 1. The comparison of the PA gain and maximum achievable and practical PA efficiencies has been performed according to Ref. [5]. The reason why the expected oscillator RF/dc efficiencies are lower is that practical oscillators contain lossy SAW resonators, matching and load coupling networks such as Wilkinson power splitters [1]. In a FLSO, 50% or more of the power may be dissipated in the two-port SAW device and other passive networks. This limits the practical FLSO efficiency to about 50%. NRO may achieve somewhat higher efficiencies since they use single-port SAW devices featuring much lower loss compared to 2-port devices [8].

TABLE I
EXPECTED NOISE REDUCTION AND EFFICIENCY OF SAW/STW OSCILLATORS USING NONLINEAR SUSTAINING AMPLIFIERS

Class	A	AB	B	C
Conduction angle θ	2π	$\pi<\theta<2\pi$	π	$0<\theta<\pi$
Amplifier gain	high	medium	low	lowest
Expected noise reduction (NR)	0	< 6dB	6 dB	6 to 25 dB
Maximum achievable PA efficiency	50%	50-78.5%	78.5%	100%
Practical PA efficiency	5-25%	25-50%	30-60%	50-85%
Expected oscillator efficiency	<10%	10-25%	25-40%	40-60%

C. The Mechanism of Bias Self Alignment and Self Limiting

If the basic PA amplifier circuit from Fig. 1 is used as a self limiting sustaining amplifier in an oscillator circuit, then, during start up, its input will be driven by the increasing amplitude of the oscillation signal. Since there is no resistor in the collector-emitter branch to perform the current self limiting function, with this circuit, it is difficult to establish A-class steady-state operating conditions. However, if the transistor is forward biased at turn on, then, according to Fig. 2 a), it will operate as a linear A-class amplifier during the time over which oscillation builds up and the amplitude of the oscillating signal is still small, as shown in [6]. The gain will be high (see Table 1) and a high average collector current will flow until the peak-to-peak drive voltage at the transistor's base reaches 1.4Vpp. Then, the base-emitter diode will start rectifying the drive signal by cutting off part of the negative half cycle which, in turn, will reduce the conducting part of the duty cycle and will move the conduction angle from A-class to AB-, B- or even C-class operating conditions, as shown in Fig. 2 b), c) and d). Thus a substantial reduction in average collector current and PA gain, compared to A-class start-up conditions, will take place. The process of current reduction will continue until the output peak voltage of the oscillation signal reaches the supply voltage level Us and locks to it. In that condition, saturation takes place, the bias self alignment process is completed and the collector current, efficiency and gain are stabilized [5]. The oscillator has reached its steady-state condition.

D. The Conduction Angle at Steady State

To make an estimate of the phase noise reduction as a result of the nonlinear PA operation, a knowledge of θ and the actual class of sustaining amplifier operation at steady state is necessary (see Table 1). Whether the oscillator will operate in the AB-, B or C-class condition, will depend on several factors such as the initial bias current, the amount of gain compression, the supply voltage at a certain loop loss and the matching conditions at the PA input and output which will not only determine the loop loss but also the shape of the input and output waveforms [13]. All these factors strongly depend on each other and their behavior is generally difficult to predict, unless accurate nonlinear simulation of the oscillator wave forms is performed. Also, the small value of θ alone is not a guarantee for low phase noise if, for example, the amount of gain compression is too high [14] or if matching is poor and the waveforms are not well behaved and very distorted. The oscillator designer should aim at minimizing the conduction angle and maximizing oscillator efficiency while keeping the gain compression and the harmonic content as low as possible [2]. PSPICE simulation is highly recommended.

In a practical oscillator, the actual value of θ can be obtained in a fairly simple collector current measurement which becomes evident from Fig. 2 a) through c). For oscillation to start, the sustaining amplifier needs to be biased at a certain collector current $I_c=I_{cbias}$ as shown in Fig. 2 a). In most cases, at start up, before oscillation has built up, I_{cbias} needs to be fairly high in order to provide sufficient drive level for AB, B or C class of

operation. After turn on, a θ proportional reduction of the average collector current will take place when steady-state conditions are established, as illustrated by Fig. 2 b), c) and d). The actual steady state conduction angle θ_{ss} in radians will be:

$$\theta_{ss} = 2\pi(I_{css}/I_{cbias}), \quad (1)$$

where I_{css} is the average collector current measured at steady state. Both currents are measured with a dc ampere meter. To measure I_{cbias}, one needs to force oscillation to stop. This can be done by breaking the loop or loading the circuit until oscillation collapses. Care should be taken not to exceed the maximum power rating of the transistor in this measurement.

E. Phase Noise Estimate during Oscillator Optimization

In the process of practical oscillator optimization, it is necessary to monitor the phase noise and make a quick estimate of whether phase noise has improved or not. Correct phase noise measurements are tedious and time consuming, and, therefore, totally inappropriate for the process of oscillator optimization. However, if one or a few phase noise data points are known, then keeping in mind that SAW oscillators typically follow a 30 dB/decade phase noise slope until the thermal noise floor is reached [1], one can make a quick estimate of the actual noise after a certain optimization step. Such an estimate can be made with a spectrum analyzer (SA) featuring low-noise synthesized local oscillators and signal-to-noise ratio measurement capability [7]. In this measurement, one has to make sure that the SA system noise floor is lower than the phase noise of the oscillator under test. The easiest way to verify this is by measuring the SA system floor with a reference oscillator, such as synthesizer, featuring much lower phase noise than the SA local oscillators and oscillator under test and then comparing the close-in noise spectrum of the measurement signal with the system floor. Fig. 3 is the close-in SA system noise floor at 10 MHz measured with a 10 MHz crystal oscillator with a phase noise by at least 20 dB lower than that of the SA local oscillators. The system floor is -113 dBc/Hz at 1 KHz carrier offset and was found to be nearly the same over the entire SA frequency range. The plot in Fig. 3 contains also the SA thermal noise floor, measured without input signal. It is by 5 dB lower than the SA system floor at 1 KHz offset, meaning that it has a negligible influence on the measurement result [7].

Fig. 4 is the close-in phase noise of a 1 GHz STW oscillator which is only about 1.5 dB higher and very close to the SA system floor. If the system floor is higher than the phase noise of the oscillator under test, then a measurement at an overtone will improve sensitivity. Fig. 5 is the close-in phase noise plot of 915 MHz STW oscillator measured at its 3-rd overtone. The phase noise suppression at 1 KHz carrier offset is -107 dBc/Hz at the 3-rd overtone frequency of 2.75 GHz and by about 5 dB higher than the system floor. The actual phase noise at the 915 MHz fundamental frequency will be by 20log(3)≈10dB lower, where 3 is the overtone number. The -117dBc/Hz phase noise suppression at the fundamental

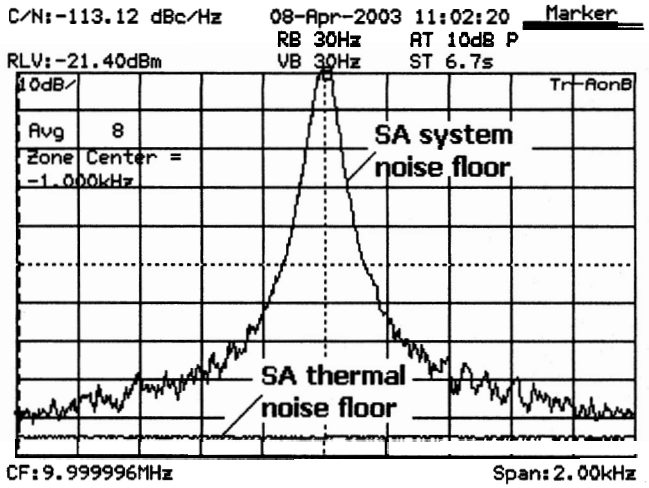

Fig. 3. SA system noise floor measured over a 2 KHz span with a 10 MHz reference with a phase noise much lower than that of the SA local oscillators.

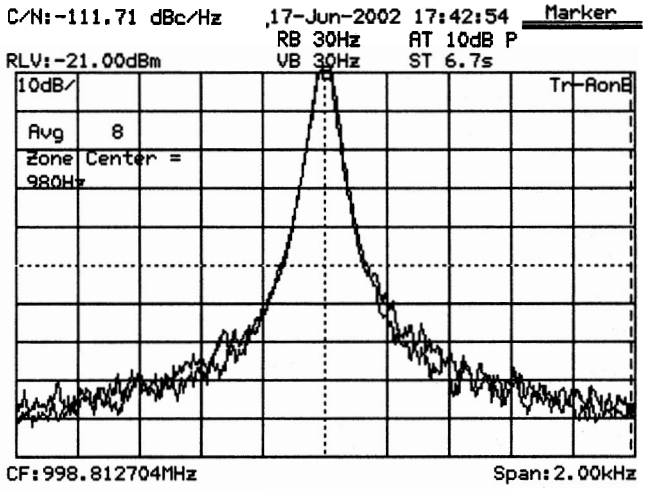

Fig. 4. Phase noise of a 1 GHz STW oscillator (upper plot) compared with the system floor (lower plot).

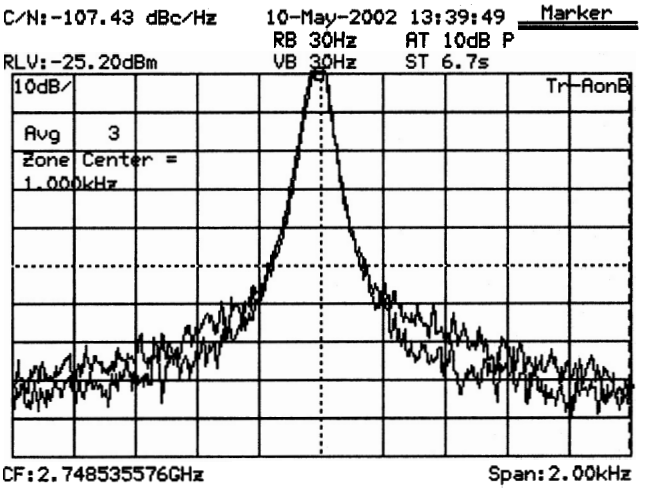

Fig. 5. Phase noise of a 915 MHz STW oscillator measured at its 3-rd overtone (upper plot) and compared with the system floor (lower plot).

frequency is clearly below the -113dBc/Hz system floor (see Fig. 4). This makes a correct measurement at the fundamental frequency impossible.

It is important to note that a correct comparison of the system floor with the measured narrowband noise spectrum requires the levels of the reference source and the device under test to be identical. Also note that the SA sensitivity can be increased significantly if the SA is driven into saturation without driving the SA mixer into saturation [7]. This is done by attenuating the measurement signal appropriately, bringing it to the reference level and decreasing that level by 10 dB as shown at the top of Fig. 3, 4 and 5. The reference level in Fig. 4 is -21 dBm while the actual signal level is -11 dBm. This means that the SA has been driven 10 dB into saturation without mixer overload alert.

III. The Oscillators

The proposed phase noise reduction principle, described in Section II, has been verified in most commonly used SAW/STW oscillator designs including NRO stabilized with single-port resonators and FLSO stabilized with low-loss and high-loss two-port resonators.

A. The surface wave devices used

The well known equivalent electrical circuits of the two-port and single-port devices, as used in the PSPICE simulations, are shown in Fig. 6 a) and b), respectively. The STW devices, used in all test oscillators, are characterized in Fig. 7, 8 and 9. The resonators' equivalent circuit parameters (ECP), according to Fig. 6, have been extracted with sufficient accuracy from simple transmission and Pi-circuit measurements as described in [8] and [9]. The 915 MHz two-port STW resonator from Fig. 7 was used in low-power and high-power single transistor based FLSO. The single-port 915 MHz STW device from Fig. 8 was implemented in a class-C

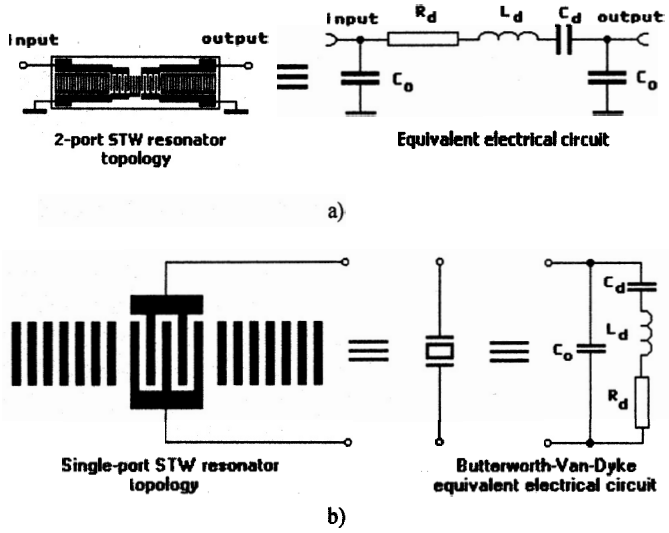

Fig. 6. Equivalent electrical circuits of the a): two-port STW resonators and b): single-port STW resonators used.

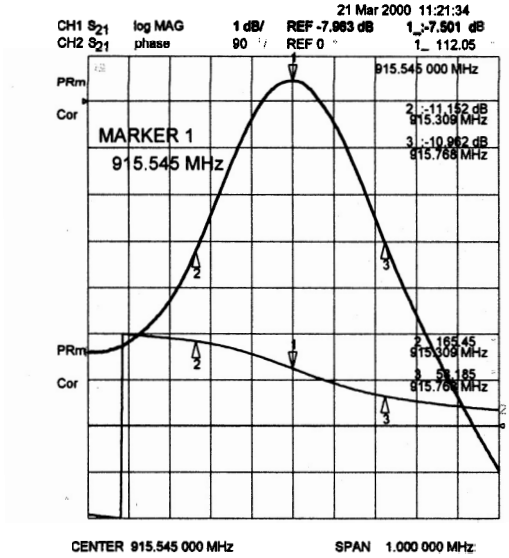

Fig. 7. Narrowband frequency and phase responses of the 2-port 915 MHz STW resonator. With a loaded and unloaded Q: Ql=2300 and Qu=3960, respectively, the ECP according to Fig. 6 a) are: Rd=138Ω; Ld=95 μH; Cd=0.318 fF; Co=2.1 pF.

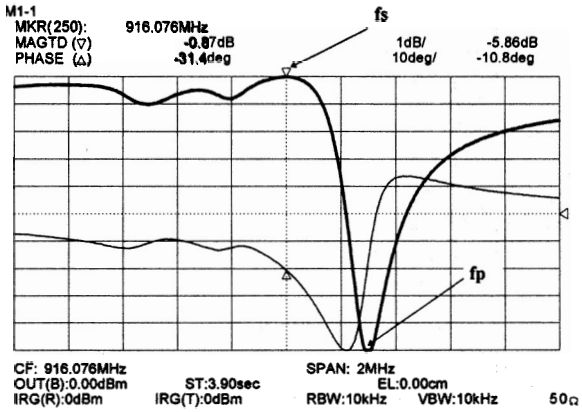

Fig. 8. Pi-circuit measured frequency and phase responses of the single-port 915 MHz STW resonator. With Q=7180, the ECP according to Fig. 6 b) are: Rd=8.3 Ohm; Ld=10.356 μH; Cd=2.915 fF; Co=4.51 pF.

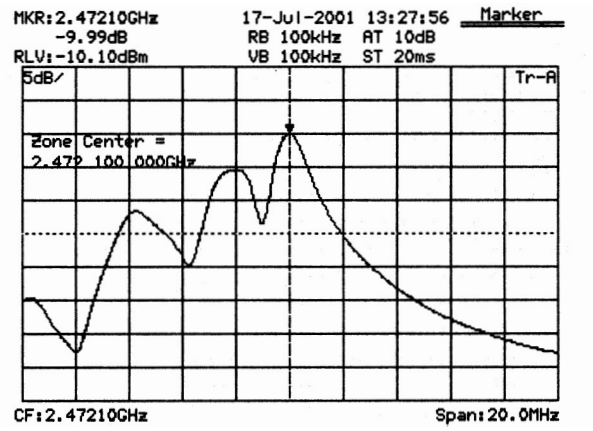

Fig. 9. Broadband frequency response of the 2-port 2.48 GHz STW resonator. With Ql=3045 and Qu=4460, the ECP, according to Fig. 6 a), are: Rd=215 Ohm; Ld=61.734 μH; Cd=0.06714 fF; Co=1.45 pF.

power NRO and the lossy 2.47 GHz device from Fig. 9 was used in a FLSO with a high-gain two-transistor based nonlinear sustaining amplifier.

B. The 915 MHz feedback loop Class-C STW oscillators

The simplified circuit diagram of the basic 915 MHz FLSO circuit, stabilized with the two-port device from Fig. 7 and optimized for low-power operation, is shown in Fig. 10. The nonlinear sustaining amplifier is realized with a single 100 mW low-cost transistor T1 which provides sufficient gain to compensate for the 7.5 dB STW device loss and for the losses in the matching networks. The initial bias current, necessary for the oscillator to start, is adjusted with the Rkb resistor. The input matching network (Cmin1, Cmin2 and Lmin) and the output matching network (Lmout1, Cmout1, Lm2 and Cout) have been carefully optimized for minimum reflections of the oscillating signal around the loop and maximum power transfer to the load resistor Rload. This is achieved by monitoring the waveforms at the collector (across Lchoke) and load (across Rload). An indication of optimum matching at a given value of Rkb is the maximum RF/dc efficiency at a minimum conduction angle. This condition is illustrated in Fig. 11 which contains the PSPICE simulated collector waveform, proportional to the oscillating collector current, and the output waveform across Rload. The sharp peaks of the collector waveform correspond to a θ value of about 15% of the duty cycle, clearly indicating C-class of transistor operation. The negative peaks below the base line are attributed to energy storage effects in the transistor [5]. The output waveform is nearly sinusoidal which is attributed to the filtering function of the output matching network. The slight distortion on that waveform is due to not sufficient harmonic suppression by the output matching network. The low-power FLSO from Fig. 10 was found to provide 9 mW of load power at a RF/dc efficiency of 41%. The phase noise suppression at 1 KHz carrier offset, measured at the 3-rd overtone was -117 dBc/Hz (see Fig. 5).

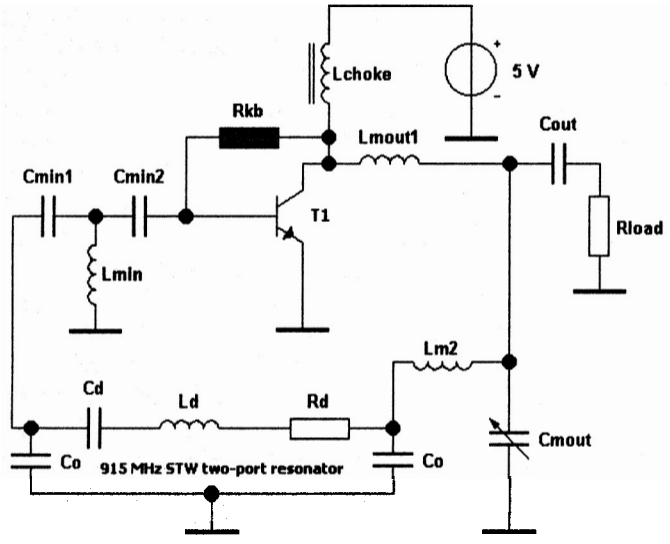

Fig. 10. Simplified circuit of the low-power single-transistor based FLSO.

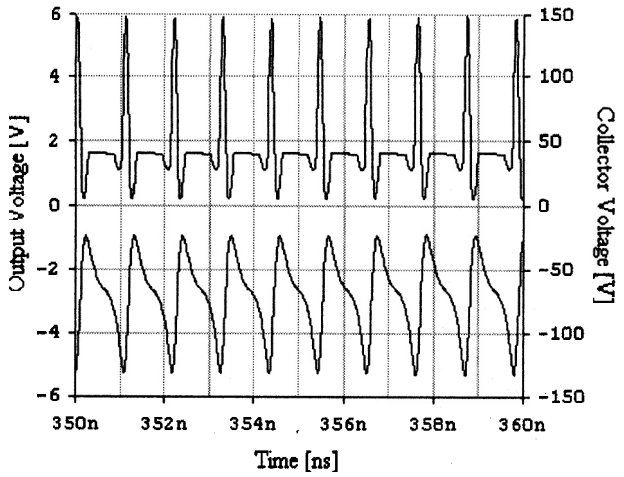

Fig. 11. Collector (upper curve) and output (lower curve) waveforms of the low-power FLSO from Fig. 10.

In a second experiment, the inductor Lchoke in Fig. 10 was replaced by a current limiting ohmic resistor and the transistor was biased at the same initial collector current and the same 5V collector-emitter voltage to achieve class-A operating conditions. No other changes to the circuit were made. The PSPICE simulated collector waveform in this case (not shown here) was much closer to sinusoidal and θ was 360 deg. The phase noise was degraded to -100 dBc/Hz which is consistent with the data from Table 1 and verifies a θ proportional sustaining amplifier 1/f noise contribution.

In another experiment, T1 from Fig. 10 was replaced with a 500 mW device, the initial bias current was increased by reducing Rkb and the input and output matching networks were optimized for the new transistor impedances. The result was an increased 200 mW output RF power and a decreased θ of about 30% at optimum matching. As a result of that, a slightly reduced efficiency of 34% and a 6 dB phase noise degradation (-111 dBc/Hz) was measured.

C. The class C negative resistance STW oscillators

SAW/STW based NRO take advantage of the much higher oscillator Q achievable with single-port resonators [8]. Excellent phase noise performance and a high RF/dc efficiency are achieved with fairly simple circuits [10]. Linear NRO circuit simulation [11] is required to achieve stable single-mode operation and optimum oscillator performance [10]. Fig. 12 a) and b) show the simplified circuit and PSPICE simulated waveforms, respectively, of a 915 MHz NRO, stabilized with the single-port STW device from Fig. 8, and using a C-class operating transistor as a sustaining amplifier. At a certain collector current, adjusted with Rkb, the single-port resonator, in parallel with Re, and the base-emitter capacitor Cbe, provide a sufficient amount of negative resistance over the narrow bandwidth of the acoustic device to compensate for the losses in the series tank (Lin, Cin), and allow oscillation to start [10]. The high-value inductors Lchoke1 and Lchoke2 do not influence oscillation conditions but eliminate dc current limiting to allow C-class operation. Finally, the output filter (Lmout and

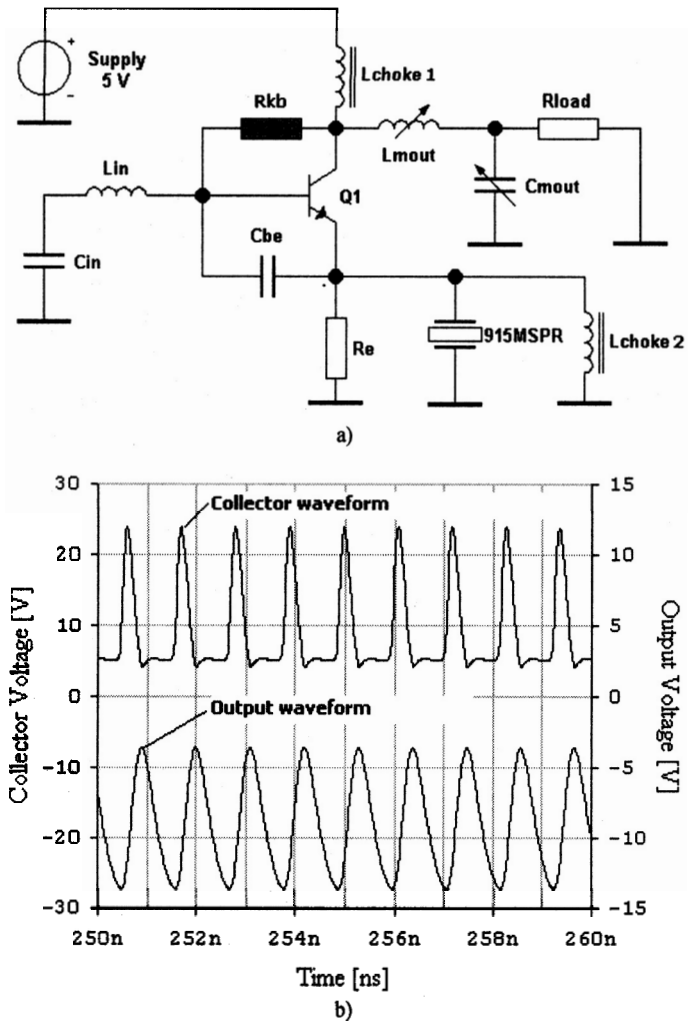

Fig. 12. C-class operating 915 MHz NRO: a): simplified circuit and b): PSPICE simulated waveforms.

Cmout), optimized using C-class amplifier design techniques [13], provides maximum RF power transfer to the load resistor while filtering the harmonics. The collector and output waveforms are very well behaved (see Fig. 12 b)). With a θ of about 35%, 100 mW output power and 38% RF/dc efficiency, this bias self aligning NRO was found to provide a remarkable -119 dBc/Hz phase noise suppression at 1 KHz carrier offset. About 10 dB phase noise degradation was the result of A-class operation in the same circuit.

An even further phase noise reduction was achieved by applying an externally variable stiff bias as shown in Fig. 13 a), thus achieving a further θ reduction as shown by the collector waveform in Fig. 13 b). To establish this condition, a variable dc bias voltage was applied to the transistor base through Lchoke3. This allows external control over θ at steady state and avoids oscillation to influence the bias conditions. As a result of the stiff bias, θ_{ss} was reduced to about 25% (see Fig. 13 b)) and the phase noise became so low that the system floor was dominating the oscillator noise even at the 3-rd highest measurable overtone. A further conduction angle reduction was not possible since, due to the absence of negative dc feedback in the circuit from Fig. 13 a), its thermal stability was very poor and no stable operation was possible. As shown in [11], the thermal stability problem could be solved with an active biasing circuit but, probably, at the expense of some noise degradation from external active components [3].

D. Two-stage sustaining amplifier based 2.48 GHz FLSO

In many SAW/STW oscillator designs, especially above 2 GHz, the acoustic devices (delay lines, two-port resonators or narrowband filters) may be quite lossy (see Fig. 9). In such cases, a single RF transistor may not provide sufficient gain and two-transistor designs may be necessary. To exert control over each of the two transistor stages in a selflimiting AB-, B or C-class sustaining amplifier becomes a serious problem since an increase in signal amplitude in one of the transistor stages will shift the conduction angle of the other and vice versa. However, if one of the transistor stages is operated at a low conduction angle and performs the selflimiting function, while the other is A-class operated and far below saturation, then, as shown in

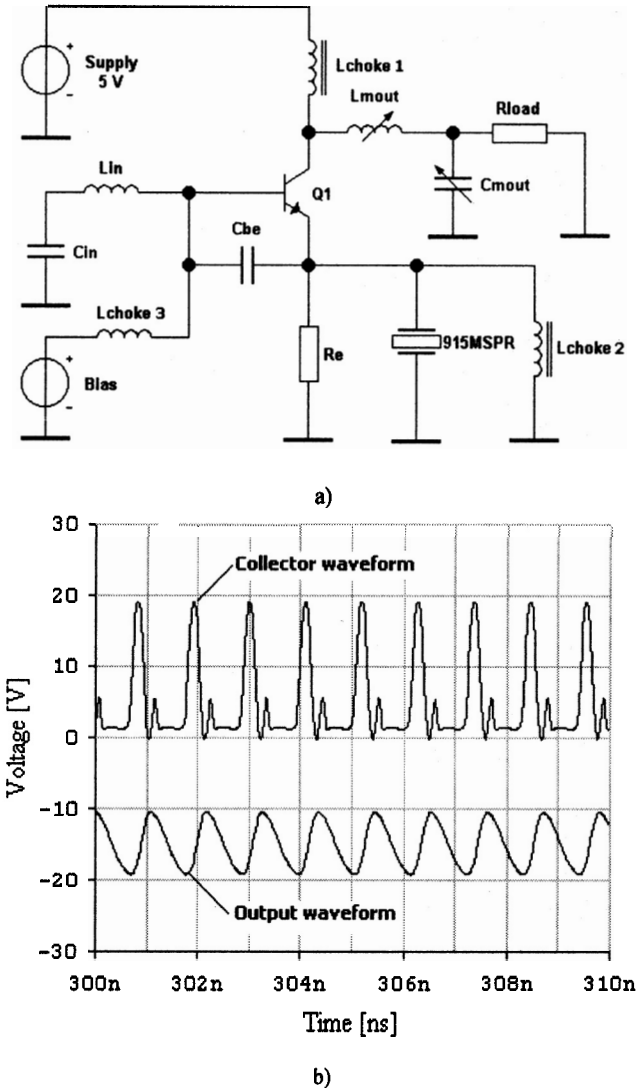

Fig. 13. Stiff bias operating C-class NRO with reduced conduction angle: a): simplified circuit and b): PSPICE simulated waveforms.

[12], a significant noise reduction should be expected compared to both transistors operating in the full conducting A-class mode and driven into voltage saturation which is often the case in designs using multiple-transistor modular amplifiers. In the 2.47 GHz FLSO circuit from Fig. 14, stabilized with the STW device from Fig. 9, the first transistor T1 is operated at a minimum conduction angle, optimized by a proper selection of the resistors Rk1 and Rkb1 at a given supply voltage. By reducing the collector-emitter bias voltage of T1 to a relatively low value (in the 0.8 to 1.5V range), the signal amplitude at test point 1 (TP1) remains constant even at a fairly large variation range of the input level at the base. In this way, T1 performs a well behaved self limiting function while the conduction angle remains fairly low, in this case, about 50% (B class), as evident from the collector waveform at TP1 in Fig. 15. Once safe selflimiting is established by T1, T2 can be biased with Rkb2 at a collector current providing a highly linear A-class operation and below voltage saturation, even without using a current limiting collector resistor. This is of great advantage if a low supply voltage is required, e.g. 3.3V in 2.488 GHz VCSO for optical communications [2]. In such cases, the inductor Lk can be used instead of a collector resistor to provide a fairly large signal level at TP2 while reducing heat dissipation and increasing efficiency. The collector waveform of T2, measured at TP2, is free from distortion indicating linear class A operation of T2.

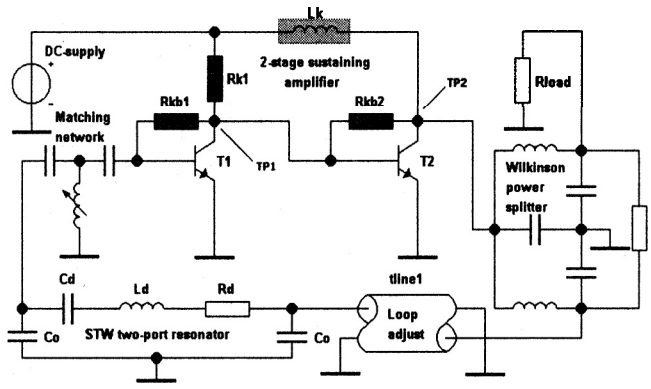

Fig. 14. Two-transistor based 2.47 GHz FLSO.

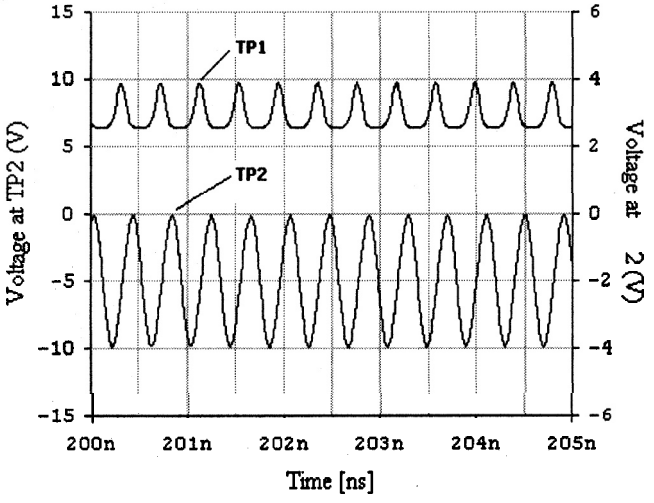

Fig. 15. PSPICE simulated collector waveforms at test points TP1 and TP2 in the circuit from Fig. 14.

When operated from a 3.3V dc supply voltage, the 2.47 GHz FLSO circuit from Fig. 14 was found to provide 4 mW of output power at a RF/dc efficiency of 5%. Compared to the other designs, the efficiency is greatly reduced. This is attributed to the fairly high 10 dB loss of the acoustic device, nearly 4 dB loss in the Wilkinson power splitter and the function of the transistor T1 which provides limiting but an insignificant contribution to the overall output power. The phase noise at 1 KHz carrier offset was measured as -103 dBc/Hz. A 7 dB degradation in phase noise performance was obtained when both transistors were biased for the full conducting voltage self limiting A-class of operation.

IV. Summary and Conclusions

This work has verified experimentally that in SAW/STW oscillators in which the active circuit is the dominant source of 1/f noise, the flicker noise contribution of Si-bipolar transistor based selflimiting sustaining amplifiers is proportional to the current conduction angle of the transistors and can be significantly reduced if one of the nonlinear AB, B or C classes of reduced conduction angle operation are used. This technique was applied to single-transistor based feedback-loop and negative-resistance STW oscillator designs, stabilized with low-loss two-port and single-port resonators in the 900 MHz range, and to two-transistor designs using lossy two-port STW devices in the 2.5 GHz range. The results indicate a substantial improvement in close-in oscillator phase noise compared to the full conducting voltage limiting A-class sustaining amplifier operation. In addition, as a result of the high efficiency of nonlinear amplifiers, output power is increased and heat dissipation is decreased.

Acknowledgment

The author wishes to gratefully acknowledge LG Precision in Seoul, Korea and Fujitsu Laboratories in Akashi, Japan for fabricating and providing the 915 MHz and 2.47 GHz STW devices, respectively, that were used in this study.

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